12/06/2002 09/992,387

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SYSTEM:OS - DIALOG OneSearch
File 348:EUROPEAN PATENTS 1978-2002/Jun W01
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File 349:PCT FULLTEXT 1983-2002/UB=20020606,UT=20020530
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12/06/2002 09/992,387

Set	Items	Description
S1	427	((BALL()GRID OR BGA OR LAND()GRID OR PAD()GRID OR PIN()GRID)(3N)ARRAY? ?)/TI,AB,CM
S2	167	(INTERCONNECT??????(3N)DENSIT?????)/TI,AB,CM
S3	6542	(100(W)(MU OR MICRON? ?))/TI,AB,CM
S4	21707	(INTEGRAT??????(2N)(CIRCUIT??? OR IC))/TI,AB,CM
S5	5031	(ELECTRIC???(3N)(COUPL??? OR CONNECT??? OR LINK??? OR JOIN???)(3N)(MEMBER? ? OR UNIT? ? OR PART? ?))/TI,AB,CM
S6	545	INTERPOSER? ?/TI,AB,CM
S7	98236	(POLYIMIDE? ? OR POLYIMIDO OR RESIN OR EPOX??? OR (HEAT??? OR WEAR OR CORROSION???)(4N)RESIST???????)/TI,AB,CM
S8	542	((GOLD OR AU)(5N)(BALL? ? OR BUMP? ?))/TI,AB,CM
S9	58	((NICKEL OR NI)(5N)(BALL? ? OR BUMP? ?))/TI,AB,CM
S10	9	((PALLADIUM OR PD)(5N)(BALL? ? OR BUMP? ?))/TI,AB,CM
S11	711	(FLIP()CHIP OR FLIP()BOND)/TI,AB,CM
S12	13416	(ENCAPSULAT?????? OR CAPSULAT?????? OR ENCAPSULANT????)/TI,AB,CM
S13	7308	(THERMOSETTING? ? OR THERMOPLASTIC???(3N)(BLEND??? OR MIX OR MIXTURE OR MIXING))/TI,AB,CM
S14	70	S1 AND S12
S15	47	S14 AND S4
S16	18	S15 AND S7
S17	1	S16 AND S8
S18	1	S16 AND S9
S19	0	S18 NOT S17
S20	3	S16 AND S11
S21	2	S20 NOT S17
S22	17	S13 AND S5
S23	0	S22 AND S2
S24	1	S22 AND S1
S25	7	S6 AND S3
S26	1	S25 AND S11
S27	0	S26 NOT S18,S21,S24
S28	1	S25 AND S12
S29	0	S28 NOT S18,S21,S24
S30	138	S5 AND S4
S31	5	S30 AND S1
S32	5	S31 AND (S8 OR S9 OR S10 OR SOLDER???)

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21/PN,PD,PR,TI,K/1 (Item 1 from file: 349)

DUAL-DIE **INTEGRATED CIRCUIT** PACKAGE
Patent and Priority Information (Country, Number, Date):
Patent: WO 200143193 A2-A3 20010614 (WO 0143193)
Priority Application: US 99458264 19991209

English Abstract
A dual-die **integrated circuit** package (10) having two **integrated circuit** chips (14, 16) **"flip chip"** attached to each other and with one of the chips (14) being aligned at a specified angle in relation to the other chip (16) to...

Claim
1 A dual-die **integrated circuit** package comprising:
a flat die-attachment surface having a plurality of external electrical contacts for connecting the package to external circuits,
a first IC chip...

...the first surface of the first IC chip remaining uncovered and electrically connected to the external electrical contacts of the die-attachment surface, and an **encapsulant** material enclosing the first and second IC chip and covering a portion of the die attachment surface such that the plurality of electrical contacts remain at least partially uncovered.

11 The **integrated circuit** package of claim 1, wherein the die-attachment surface is a part of a **ball grid array** type structure and includes a series of solder bumps on a bottom surface of the chip package. -12

15 The method of forming a dual-die **integrated circuit** package, as in claim 14, wherein the step of connecting the second chip to the first chip is carried out by using an anisotropic **epoxy**.

21/PN,PD,PR,TI,K/2 (Item 2 from file: 349)

METHOD OF INCREASING PACKAGE RELIABILITY BY DESIGNING IN PLANE CTE GRADIENTS

Patent and Priority Information (Country, Number, Date):
Patent: WO 9820556 A1 19980514
Priority Application: US 96745597 19961108

.. Figure 20 is a SEM image showing the node-fibril infrastructure of an ePTFE matrix used in another embodiment of the present invention.
I Adhesive **Encapsulation**
For a more complete understanding of the invention, attention is directed to FIGS. 1 and 2, in which a chip/package system 10 includes a package 12 having first and second opposite planar surfaces 14 and 16. An **integrated circuit** chip 18 is connectable through solder bumps or ...center of core layer 52 through which a plane of symmetry passes:
a) 20grn Cu/Ni/Au layer 56, a conductor;
b) 44grn cyanate ester-**epoxy**-ePTFE (CE/E-ePTFE) layer 58, a dielectric;
Referring again to Figures 1 and 2, an **integrated circuit** chip, such as chip 18, is typically made of a material, such as silicon, that has a substantially different coefficient of thermal expansion (CTE) as...Average CTE for the entire package 12. The use of a different CTE for a chip-underlying portion of a package is particularly suited for **flip chip** packages or others employing peripheral **ball grid array** connectors between the package and the PWB. As seen in Figure 2, solder balls are not used between the PWB 40 and the package 12...volume of at least 30%, preferably at least 50%, and most preferably at least 70%, and facilitates the impregnation of thermoset or -28 thermoplastic adhesive **resin** and particulate filler paste in the voids while providing a ...the fillers. The adhesive itself may be a thermoset or thermoplastic and can include polyglycidyl ether, polycyanurate, polyisocyanate, bis-triazine resins, poly (bis-maleimide), norborneneterminated **polyimide**, polynorbornene, acetylene-terminated **polyimide**, polybutadiene and functionalized copolymers thereof, cyclic olefinic polycyclobutene, polysiloxanes, poly 0 sisqualoxane, functionalized polyphenylene ether, polyacrylate, novolak polymers and copolymers, fluoropolymers and copolymers, melamine polymers ...5, Nelco Corp.) in IVIEK The dispersion was constantly agitated so as to insure uniformity. A swatch of expanded PTFE was then dipped into the **resin** mixture. The web was dried at 1651C for 1 min. under tension to afford a flexible composite. The partially-cured adhesive composite thus produced comprised of 57 weight percent TiO2, 13 weight percent PTFE and 30 weight percent **epoxy** adhesive. Several plies of the adhesive sheet were laid up between copper foil and pressed at 600 psi in a vacuum-assisted hydraulic press at...

...HW-1 1-89, Harbison Walker Corp.) which was pretreated with phenyltrimethoxysilane (04330, Huls/Petrarch) into a manganese catalyzed solution of 200 g bismaleimide triazine **resin** (BT206OBJ, Mitsubishi Gas Chemical) and 388 g MEK. The dispersion was constantly agitated so as to insure uniformity. A swatch of 0.0002" thick expanded PTFE was then

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24/PN,PD,PR,TI,K/1 (Item 1 from file: 348)
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Plastic molded pin grid chip carrier package.
Gegossenes Kunststoff-Chip-Gehause mit Steckermuster.
Boitier moule en matiere plastique avec grille de fiches pour dispositif a circuits integres.
PATENT (CC, No, Kind, Date): EP 268181 A1 880525 (Basic)
EP 268181 B1 920729
PRIORITY (CC, No, Date): JP 86272190 861115; JP 86272191 861115

...ABSTRACT An improved plastic molded chip carrier package for a semiconductor chip (1,40) has a plurality of I/O pins (20,60) arranged on a **pin grid array**. The **pin grid array** comprises at least two row of the I/O pins (20,60) disposed along the sides of the chip (1,40) in such a manner...

...CLAIMS chip carrier package as set forth in claim 1, wherein each I/O pin has its top projecting above the top surface of the carrier **member** for **electrical connection** with said chip by means of a wire element.
3. A plastic molded chip carrier package as set forth in claim 1, wherein the I...

...chip carrier package as set forth in claim 1, further including a transparent covering material which is placed on the top surface of the carrier **member** for sealing the chip and its **electrical connection** to the I/O pins.
5. A plastic molded chip carrier package as set forth in claim 4, wherein said transparent covering material is a...

...row.
7. A plastic molded chip carrier package as set forth in claim 6, wherein said plastic substrate is a thin plate made from a **thermosetting** resin.
8. A plastic molded chip carrier package as set forth in claim 6, wherein each of said conductor lines is formed with a solder...

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32/PN,PD,PR,TI,K/3 (Item 1 from file: 349)
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CONTROLLED COMPLIANCE FINE PITCH INTERCONNECT
Patent and Priority Information (Country, Number, Date):
Patent: WO 200109980 A2-A3 20010208 (WO 0109980)
Priority Application: US 99146825 19990802
...a printed circuit probe is also disclosed. The second circuit member can be a printed circuit board, another flexible circuit, a bare-die device, an **integrated circuit** device, an organic or inorganic substrate, a rigid circuit and virtually any other type of electrical component. A plurality of electrical contacts are arranged in...

...housing acts as a receptacle to individually locate and generally align the electrical contacts, while preventing adjacent contacts from touching. The first ends of the **electrical** contacts are electrically **coupled** to a flexible circuit **member**. The **electrical** contacts are free to move along a central axis within the housing. The second ends of the electrical contacts are free to electrically couple with one or more second circuit members without the use of **solder**.
Pin-type connectors **soldered** into plated through holes or vias are among the most commonly used in the industry today. Pins on the connector body are inserted through plated holes or vias on a printed circuit board and **soldered** in place using conventional means. Another connector or a packaged semiconductor device is then inserted and retained by the connector body by mechanical interference or friction. The tin lead alloy **solder** and associated chemicals used throughout the process of **soldering** these connectors to the
printed circuit board have come under increased scrutiny due to their environmental impact. Additionally, the plastic housings of these connectors undergo a significant amount of therinal activity during the **soldering** process, which stresses the component and threatens reliability.
electrically couple ...bias on the electrical contacts 588. Singulations 602 in the flexible circuit member 584 facilitate movement of the electrical contacts 588 within the substrate 582. **Solder** balls 594 electrically couple with BGA contact pads 586 on the flexible circuit member 584.
I An electrical connector for electrically interconnecting terminals on a flexible circuit member with terminals on a second circuit **member**, the **electrical connector** comprising:
a housing having a plurality of through holes extending between a first surface and a second surface, each of the through holes defining
2 The **electrical connector** of claim 1 wherein the resilient **member** comprises a compliant encapsulating material interposed between a
portion of the through hole and a portion of the **electrical** contacts.

10 The **electrical connector** of claim I wherein the second ends of the electrical contacts are capable of engaging with a connector member selected from the group consisting of a flexible circuit, a ribbon

connector, a cable, a printed circuit board, a ball gri'd **array** (**BGA**), a **land grid array** (LGA), a plastic leaded chip carrier (PLCQ, a pin gri'd array (PGA), a small outline **integrated circuit** (SOIC), a dual in-line package (DIP), a quad flat package (QFP), a leadless chip carrier (LCQ, a chip scale package (CSP), or packaged or unpackaged **integrated circuits**.

..with a second circuit member selected from the group consisting of a flexible circuit, a i bon connector, a cable, a printed circuit board, a **ball grid array** (**BGA**), a rib **land grid array** (LGA), a plastic leaded chip carrier (PLCC), a **pin grid array** (PGA), a small outline **integrated circuit** (SOIC), a dual in-line package (DIP), a quad flat package (QFP), a leadless chip carrier (LCC), a chip scale package (CSP), packaged and unpackaged **integrated circuits**

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32/PN,PD,PR,TI,K/4 (Item 2 from file: 349)
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MULTI-MODE COMPLIANT CONNECTOR AND REPLACEABLE CHIP MODULE UTILIZING THE SAME
Patent: WO 9850985 A1 19981112
Priority Application: US 97852116 19970506; US 97955563 19971017; US 9763927 19971031

English Abstract
An **electrical connector** for electrically **connecting** a first circuit **member** to a second circuit **member**. The **electrical connector** includes an electrically insulative **connector** housing having one or more apertures. A first contact member is located in the aperture. The first contact member has a first circuit interface portion...

Pin-type connectors **soldered** into plated through holes or vias are among the most commonly used in the industry today. Pins on the connector body are inserted through plated holes or vias on a printed circuit
board and **soldered** in place using conventional means. Another connector
or a packaged semiconductor device is then inserted and retained by the connector body by mechanical interference or ffiction. The tin lead alloy **solder** and associated chemicals used throughout the process of **soldering**
these connectors to the printed circuit board have come under increased scrutiny due to their environmental impact. The plastic housings of these connectors undergo a significant amount of thermal activity during the **soldering** process, which stresses the component and threatens reliability.
The **soldered** contacts on the connector body are typically the means of supporting the device being interfaced by the connector and are subject to fatigue, stress deformation, **solder** bridging, and co-planarity
I
errors, potentially causing premature failure or loss of continuity. In particular, as the mating connector or semiconductor device is inserted and
removed from the present connector, the elastic limit on the contacts **soldered** to the circuit board may be exceeded causing a loss of continuity.

Thes

An alternate electrical interconnection technique involves placement of **solder** balls or the like between respective circuit elements.
1 An **electrical connector** for electrically **connecting** a first circuit **members** to a second circuit member, comprising:
an electrically insulative connector housing having one or more apertures,

a first contact member located in the apeiture having...
11 The apparatus of claim I wherein the first circuit member is selected from a group consisting of packaged **integrated circuit** devices, unpackaged **integrated circuit** devices and a functional group of **integrated circuit** devices.
12 The apparatus of claim I wherein the first circuit interface portion is capable of engaging with a connector member selected from the group consisting of an edge card, a j-lead device, a flex circuit, a ribbon connector, a cable, a **ball grid array** (**BGA**), a **land grid array** (LGA), a plastic leaded chip carrier (PLCC), a **pin grid array** (PGA), a small
. The apparatus of claim 22 wherein the second circuit interface is selected from a group consisting of edge connectors, ribbon cables, printed **circuit** boards, **integrated circuit** devices, organic or

32/PN,PD,PR,TI,K/5 (Item 3 from file: 349)

A **BALL GRID ARRAY** STRUCTURE AND METHOD FOR PACKAGING AN **INTEGRATED CIRCUIT** CH

Patent and Priority Information (Country, Number, Date):
Patent: WO 9715076 A1 19970424
Priority Application: US 95982 19951017

English Abstract
An **integrated circuit** package (210) comprising a substrate that has a dielectric layer and a micro-filled via formed substantially in the center of a hole in the...

Detailed Description
... an IC chip 128 mounted on BGA substrate 125's first side 121 using wire bond structure 112 (FIG. 1A), and an area array of **solder** balls 122A-122J (where J is the number of balls) attached to BGA substrate 125's second side 123. BGA substrate 125 has a number of plated vias 125A-125K (where K is the number of vias) that electrically couple IC chip 128 to **solder** balls 122A 122J. BGA package 120 is typically assembled independent of, and then mounted on a structure, such as a printed circuit board 126.
The planarity is sufficient to allow various layers to be formed over a pad-on-via structure or to allow a bond wire or a **solder** ball to be attached to a pad of a pad-on-via structure, Micro filled vias in accordance with this invention can also be formed..
1 A package for supporting at least one **integrated circuit** chip, said package having a first outer surface and a second outer surface opposite said first outer surface, said package comprising: a dielectric layer located...
.outer surface, said inner layer being separated from said chip bonding pads by said dielectric layer, a trace of said plurality of traces being electrically **connected** to said **electrical** conductor, said trace being **part** of said electrical path,
..least said dielectric layer and formed on said contact side in a first predetermined configuration suitable for connection to a plurality of pads on said **integrated circuit** chip; a plurality of ball attach pads supported by at least said dielectric layer and formed on said contact side in a second predetermined configuration...